REMARKS/ARGUMENTS

Applicants received the Office action dated May 5, 2006, in which the Examiner rejected claims 1-18 under 35 U.S.C. § 102(b) as being anticipated by Harrell (U.S. Pat. No. 5,682,554, hereinafter "Harrell"). Applicants traverse all claim rejections for the reasons provided below.

Harrell purports to the solve the problem of a host computer 22 that operates with a clock frequency and that attempts to send data to a graphics processor 21 (Fig. 2) that operates in accordance with a different clock frequency. That is, the host computer may provide data to the graphics processor at a rate that differs from the rate at which the graphics processor can consume the data. See e.g., cols. 1 and 2. Harrell solves this problem by providing an interface 23 between the host computer 22 and graphics processor 21 (Fig. 2). The interface 23 contains a first in first out (FIFO) data buffer 24 and a pair of counters 25 and 26. Data is provided by the host computer on bus 40 and stored in the FIFO buffer. The graphics process extracts the data from the FIFO data buffer via bus 42.

In Harrell, it may be that the graphics processor 21 is unable to retrieve the data from the FIFO data buffer as fast as the host computer 22 is storing data into the FIFO data buffer. In this situation, the FIFO data buffer will become full. On the other hand, it may be that the host computer 22 cannot store data into the FIFO buffer as fast as the graphics controller 21 retrieves the data from the FIFO buffer. In this situation, the FIFO data buffer will become empty. Neither condition is desirable. The counter 25 will cause an interrupt to be generated to the host computer when the FIFO buffer is almost full. This interrupt will cause the host computer to cease storing data into the FIFO buffer. The counter 26 will cause an interrupt to be generated to the graphics controller when the FIFO buffer is almost empty. This interrupt will cause the graphics controller to cease trying to retrieve data from the FIFO buffer.

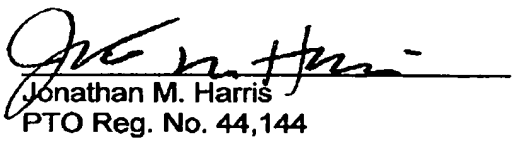
Applicants' contribution is substantially different. Claim 1, for example, requires "a processor for executing program instructions configured to programmably alter a rate at which the predetermined number of pulses are

produced by the timing logic unit, thereby adjusting an expiration period for completing a transaction cycle associated with the transaction request." The Examiner has stated that Harrell's FIFO data buffer is akin to the claimed "processor." Clearly, a FIFO data buffer, which simply stores data, is not the same as a processor that executes program instructions. Further, Harrell fails to teach or even suggest any type of logic that alters the rate at which a predetermined number of pulses are produced by timing logic to thereby adjust an expiration period. Harrell does not even teach the concept of an "expiration period" as claimed, that is, an expiration period for completing a transaction cycle associated with a transaction request. For at least these reasons, claim 1 and its dependent claims are in condition for allowance. If the Examiner continues to reject claim 1 as allegedly anticipated by Harrell, Applicants respectfully request a clearer explanation as to how the components of Harrell's interface 23 match up to the claim limitations.

Claim 8 is allowable for the same or similar reasons as claim 1. Accordingly, claim 8 and its dependent claims are in condition for allowance.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



Jonathan M. Harris
PTO Reg. No. 44,144
CONLEY ROSE, P.C.
(713) 238-8000 (Phone)
(713) 238-8008 (Fax)
ATTORNEY FOR APPLICANTS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
Legal Dept., M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400